REMARKS

Claims 1-37 are pending and stand rejected. Claims are currently amended. The Examiner's reconsideration of the rejections is respectfully requested in view of the above amendments and the following remarks.

Reopening of Prosecution/Reinstatement of Appeal

Applicants would note for the record once again that this Office Action was issued as part of a reopening of prosecution in response to Applicants' previously filed Appeal Brief. Applicants retain their right to reinstate the Appeal, without cost, in this Action in the event that the Examiner issues a Final Office Action.

Claim Rejections 35 U.S.C. 112

Claim 29 is rejected for supposedly failing to comply with the written description requirement. The Examiner contends that the specification does not support the claimed configurable memory with three modes of operation where any one of the modes is selectable at any time based on comparing an address to an address range contained in a configuration register. The rejection is traversed.

With regard to the legal issues regarding the written description requirement, the Examiner should note the following. In assessing whether a specification satisfies the "written description" requirement under 35 U.S.C. 112, first paragraph, with respect to the claimed invention(s), the fundamental factual inquiry is whether the patent specification describes the claimed invention with *reasonable* clarity such that one of ordinary skill in the art can reasonably conclude that the inventor(s) had possession of the claimed invention as of the filing date of the specification. See *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed Cir. 1991). Compliance with the written description requirement does not compel use of any particular form

of description, so long as the description clearly allows one of ordinary skill in the art to recognize that the applicant invented what is defined by the patent claims. See *In Re Alton*, 76 F.3d 1168, 1172 (Fed. Cir. 1996). Indeed, it is well established that the subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement. See *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000). "If a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate description is met." *In re Alton*, 76 F.3d at 1175 (see also *Vas-Cath*, 935 F.2d at 1563).

The Office Action does not present a prima facie case regarding the written description rejection of claim 29. There is clear support for the claimed subject matter of claim 29. For instance, the Examiner should note the following teachings in Applicants' specification, at page 15, lines 3 ~ p. 16, line 13:

> The memory configuration logic 420 is further responsible for selecting the operating mode of the configurable memory array 130. Such selection of the operating mode may be based on, for example, the memory address, mode information received in conjunction with the memory address, a configuration register, a configuration signal, and/or other control information. That is, given the teachings of the present invention provided herein, one of ordinary skill in the related art will contemplate these and various other criteria upon which selection of the operating mode of the configurable memory array 130 can be based, while maintaining the spirit and scope of the present invention.
>
> The memory configuration logic 420 includes an array address mapping module 425, a control module 430, mode selection logic 435, tag match logic 440, and multiplexers 445 and 450. The configuration of the memory array 410 is controlled by the mode selection logic 435, which generates all necessary control and configuration signals. The mode of operation can be selected by . . . a function the memory address itself. These control logic components enable, for example, four modes of operation: local memory read mode; local memory write mode; cache read mode; and cache write mode. (emphasis added)

The above teachings provide clear and explicit support for the subject matter of claim 29.

Furthermore, the subject matter of claim 29 is supported by the following teachings in Applicants' specification, at page 23, lines 3 ~ 17, and FIG. 5:

> Yet another exemplary configuration option is as follows. When the CPU 110 performs a memory access, **the access mode of the configurable memory array 130 is selected based upon the address of the memory access (step 550). For example,** when the CPU 110 performs a memory access, the supplied address of the access determines whether the memory array is to be treated as local memory or cache. This can be used to effectively partition the configurable memory array 130 into (1) a small high-speed local working memory for data processing and (2) a cache for access to a large system memory. The control information may be obtained by comparing the address to one or more address ranges contained in configuration register(s) (step 550a), or by performing any of a variety of logical operations on the address bits (step 550b).

The Examiner relies on the above teachings to find that the "specification discloses only two modes of access for any given address- cache mode access and local memory mode access." This finding is unreasonable in view of the fact that there is no limiting language in the cited passage to support a finding that the invention is limited to selection of only two different modes based on the address of the memory acess. Indeed, the cited passage cites the two different modes by way of example. In any event, the specification is replete with specific support for claim 29 (such as cited above) which clearly undermines such a restrictive finding.

Irrespective of whether or not the subject matter of claim 29 is explicitely described *in haec verba* in the specification, in order to support this 112 rejection, it is incumbant on the Examiner to explain why one of ordinary skill in the art would not reasonably conclude that the inventor(s) had possession of the claimed invention (of claim 29) as of the filing date of the specification given the broad, non-limiting teachings in Applicants specification (as cited above)

of using memory addresses for selecting multiple modes, with 2 and 4 modes as specifically described examples. Without such a showing, the 112 rejections should be withdrawn.

Claim Rejections 35 U.S.C. 102

The following anticipation rejections are asserted in the Office Action:

A. Claims 1-8, and 10-20 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,678,790 to Kumar.

B. Claims 1 and 21 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2002/0087821 to Saulsbury.

C. Claims 1, 10-14 and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,321,318 to Baltz.

D. Claims 1-3, 6-10, 13-17, 20-23, 25, 26, 29, 30 and 33 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,868,472 to Miyake.

Kumar Fails to Anticipate the Claimed Inventions

The anticipation rejections of claims 1-8 and 10-20 based on Kumar are improper as a matter of law and fact for the same reasons asserted numerous times in the previously filed Appeal brief and subsequent response, which are incorporated herein by reference.

Baltz Fails to Anticipate the Claimed Inventions

The anticipation rejections of claims 1, 10-14, and 21 based on Baltz are improper as a matter of law and fact for the same reasons asserted numerous times in the previously filed Appeal brief and subsequent response, which are incorporated herein by reference.

Saulsbury Fails to Anticipate the Claimed Inventions

At the very least, the Examiner has not fairly demonstrated how Saulsbury teaches a configurable memory comprising *a memory array in which both tag bits and data bits are stored in a single data line in the memory array*, in the first mode of operation where the configurable memory operates as a cache, as recited in claim 1. Saulsbury's general statement that a DRAM memory can be configured as "a cache memory with associated tags" does not teach or suggest *a memory array in which both tag bits and data bits are stored in a single data line in the memory array*. This generally teaching can more readily apply to associated tags that are stored in separate tag memories or libraries. In fact, FIG. 3 of Saulsbury discloses a separate caches (112) and (114) for data and tags. The teachings of Saulsbury do not support the anticipation rejection.

The Claims are Patentable over Miyake

In formulating the rejections based on Miyake, the Examiner relies on various embodiments by mixing different elements to establish anticipation. However, anticipation is not properly established in that manner. For instance, the Examiner cites the embodiment in FIG. 35 of Miyake (Col 34, lines 40-50) to show a cache portion (320) having a storage part (326) that functions as a cache memory or a random access memory. However, FIG. 37 illustrates that the tags (307) are separate from the storage part (326) when the system of FIG. 35 operates in cache mode. The Examiner instead relies on a different embodiment of FIG. 8 to shown tag and data stored in a cache lines. However, FIG. 8 illustrates a direct-mapped unified cache architecture (see, Col. 9, lines 43-44), which does not operate in different cache or RAM modes. The Examiner cannot mix elements from distinct embodiments of the Miyake reference to establish anticipation. For at least these reasons, no prima facie case of anticipation has been established for clams 1 and 30 based on Miyake.

Moreover, the claims have been amended to clarify essentially that one of multiple modes of are selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select one of the modes of operation.

In Col. 37, lines 7-47, Miyake teaches that a CPU sends control signals to set flags in the cache controller (325) so that cache ways can be configured as RAMs and to cause RAM address registers (various units (321~324)) to hold required address values that correspond to the address spaces of the cache memory 326 acting as RAMs. In this regard, Miyake does not specifically disclose *comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select one of the modes of operation,* as generally recited in claims 22, 26, 29, 30, and 33.

Accordingly, withdrawal of the anticipation rejections is requested.

Claim Rejections 35 U.S.C. 103

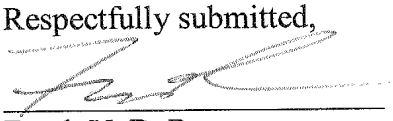
(i) Claim 24 stands rejected as being unpatentable over Miyake in view of U.S. Patent 6,377,912 to Sample, or in the alternative in view of U.S. Patent 6,611,796 to Natarajan.

(ii). Claims 27, 28, 31, 34-37 are rejected as being unpatentable over Miyake in view of U.S. Patent 6,426,549 to Isaak.

The above rejections are based in part on the primary reference as disclosing the elements of the base claims from which claims 24, 27, 28, 31 and 34-37 depend. However, the claims have been amended to further clarify the differences over Miyake. Accordingly, the obviousness rejections are improper for at least the same reasons given above with respect to the deficiencies of Miyake.

Accordingly, withdrawal of the obviousness rejections is requested.

Respectfully submitted,



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